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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,051	07/08/2003	Ming-Ren Lin	H1132	7561

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HARRITY SNYDER, LLP
11350 Random Hills Road
SUITE 600
FAIRFAX, VA 22030

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,051	LIN ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the decision by the Board of Patent Appeals and Interferences filed on 4/21/06, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

2. Note that the term "fin structure" has been interpreted in light of applicant's specification and figures as being a structure as shown in figures 3A and 3B. This interpretation is consistent with applicant's previous arguments and the decision from the Board of Patent Appeals and Interferences.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 13 – 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (USPUB 2004/0048424, Wu), with evidence provided by Wolf et al. (originally cited by Examiner in the examiner's answer mailed 9/7/05, relied upon herein as evidence).

With regard to claim 13, Wu discloses in figures 6 – 10 a method for doping fin structures in FinFET devices. Wu discloses in figure7b and paragraph [0021] forming a first glass layer (10) on the fin structures of a first area (6) and a second area (5). Wu discloses in figure 7b and paragraph [0021] removing the first glass layer from the second area. Wu discloses in figure 8b and paragraph [0022] forming a second glass layer (12) on the fin structures of the first area and the second area. Wu discloses in figure 9b and paragraph [0023] annealing the first area and the second area to dope the fin structures of the first area and the second area. In this annealing step, the "fin structure" underneath the gate is inherently doped due to lateral diffusion. The dopants inherently diffuse some amount in the lateral direction and thus will dope underneath the gate. This inherently constitutes "doping" the "fin structure" underneath the gate. See Wolf et al. as evidence of this inherent phenomenon.

With regard to claim 14, Wu discloses in figure 10 and paragraph [0024] removing the second glass layer from the first area and the second area and removing the first glass layer from the first area.

With regard to claim 20, Wu discloses in figure 7b and paragraph [0021] wherein the forming a first glass layer includes forming the first glass layer directly on the fin structures of the first area and the second area (i.e. before masking 11 and etching layer 10 from the second area).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Frenette et al. (USPAT 5770490, Frenette), with evidence provided by Wolf et al. (originally cited by Examiner in the examiner's answer mailed 9/7/05, relied upon herein as evidence).

With regard to claim 1:

Wu discloses in figures 6 – 10 a method for forming FinFET devices. Wu discloses in figure 6, figure 7a and paragraph [0019] forming a first fin structure (5), a source region, and a drain region (portions of 5 not covered by gate 9) in a first area of a wafer (1/2). Wu discloses in figure 6, figure 7 and paragraph [0019] forming a second fin structure (6), a source region, and a drain region (portions of 6 not covered by gate 9) in a second area of the wafer. Wu discloses in figure 7b and paragraph [0021] forming a boron silicate glass layer (10) on the first area and the second area. Wu discloses in figure 7b and paragraph [0021] removing the boron silicate glass layer from the second area. Wu discloses in figure 8b and paragraph [0022] forming a phosphosilicate glass layer (12) on the first area and the second area. Wu discloses in figure 9b and paragraph [0023] annealing the first area and the second area, the

annealing causing the first fin structure, source region, and drain region of the first area to be doped with boron and causing the second fin structure, source region, and drain region of the second area to be doped with phosphorus. Note that the first and second "fin" structure are inherently doped as the dopants will diffuse under the edge of the gate, thus doping a portion of the fin structures underneath the gate. See Wolf et al. as evidence of this lateral diffusion. Wu discloses in figure 10 and paragraph [0024] removing the phosphosilicate glass layer from the first area and the second area and removing the boron silicate glass layer from the first area.

As described above, Wu teaches first forming a boron silicate glass layer and then forming a phosphosilicate glass layer. Wu does not teach first forming the phosphosilicate glass layer and then, second, forming the boron silicate glass layer. It is well known in the art that when simultaneously doping source and drain regions using phosphosilicate glass and boron silicon glass the glass layers may be deposited in any order. Whether phosphosilicate glass is used first or boron silicate glass is used first, this would be recognized by the ordinary artisian as a design choice.

Frenette teaches in figures 2 – 5 and column 3, line 28 – column 4, line 10 wherein either phosphosilicate glass or boron silicate glass can be deposited first (layer 10), and the other glass layer (whichever phosphosilicate or boron silicate is not layer 10) is deposited second 34 when doping source and drain regions (40/42 and 44/46).

It would have been obvious to one of ordinary skill in the art at the time of the present invention to first deposit phosphosilicate glass as layer 10 in Wu and then deposit boron silicate glass as layer 12 in Wu in view of the teaching of Frenette in order

to use a design choice that is well understood in the art as articulated by Frenette in column 3, line 28 – column 4, line 10. Further, MPEP 2144.04 IV.C. states that changes in a sequence of adding ingredients is obvious. In this case the ingredients are the glass layers, and Frenette clearly teaches in column 3, line 28 – column 4, line 10 that they may be deposited (added) in either order to serve the same purpose of doping source drain regions.

The combination of Wu with Frenette, wherein layer 10 is phosphosilicate glass and layer 12 is boron silicate glass, will be used when considering the remainder of the claims.

With regard to claim 2, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] and [0022], wherein the forming a phosphosilicate glass layer on the first area and the second area includes depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å (the overlapping, disclosed range of 100 Å – 2000 Å anticipates the claimed range).

With regard to claim 3, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] and [0022], wherein the forming a boron silicate glass layer on the first area and the second area includes: depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å (the overlapping, disclosed range of 100 Å – 2000 Å anticipates the claimed range).

With regard to claim 4, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0023], wherein the first area is an N-channel area (when layer 10 is phosphosilicate glass).

With regard to claim 5, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0023], wherein the second area is a P-channel area (when layer 12 is borosilicate glass).

With regard to claim 6, the combination of Wu and Frenette teaches in Wu, figure7b and paragraphs [0021] – [0022], wherein the removing a phosphosilicate glass layer from the second area includes masking (11) the first area, and etching the phosphosilicate glass from the second area (when layer 10 is phosphosilicate glass).

Claims 7 – 12 will be considered using the combination of Wu and Frenette with Wolf et al. as evidence similar to the combination of Wu and Frenette used in claims 1 – 6, which, for simplicity, will not be repeated here.

With regard to claim 7, the combination of Wu and Frenette with Wolf et al. as evidence, teaches in Wu, figures 6 – 10 paragraphs [0019] – [0023], a method for doping a fin structure and source and drain regions in FinFET devices. The combination of Wu and Frenette teaches in Wu, figures 6 – 7b and paragraphs [0021] and [0023], forming a first glass layer (10) on the fin structure and source and drain regions of an N-channel device (5, in combination) and a P-channel device (6 in combination). The combination of Wu and Frenette teaches in Wu, figure 7b and

paragraphs [0021] – [0023], removing the first glass layer from the P-channel device. The combination of Wu and Frenette teaches in Wu, figure 8b and paragraphs [0021] – [0023], forming a second glass layer (12) on the fin structure and source and drain regions of the N-channel device and the P-channel device, the second glass layer being different than the first glass layer. The combination of Wu and Frenette teaches in Wu, figure 9b and paragraph [0023], annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device. As discusses above, this annealing step inherently dopes a portion of the fin structure under the gate due to lateral diffusion as evidenced by Wu et al.

With regard to claim 8, the combination of Wu and Frenette teaches in Wu, figure 10 and paragraph [0024], removing the second glass layer from the N-channel device and the P-channel device, and removing the first glass layer from the N-channel device.

With regard to claim 9, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0022], wherein the first glass layer comprises phosphosilicate glass and the second glass layer comprises boron silicate glass.

With regard to claim 10, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0022], wherein the forming a first glass layer on the N-channel device and the P-channel device includes depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å (the overlapping, disclosed range of 100 Å – 2000 Å anticipates the claimed range).

With regard to claim 11, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0022], wherein the forming a second glass layer on the N-channel device and the P-channel device includes depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å (the overlapping, disclosed range of 100 Å – 2000 Å anticipates the claimed range).

With regard to claim 12, the combination of Wu and Frenette teaches in Wu, figure 7b and paragraphs [0021] – [0022], wherein the removing the first glass layer from the P-channel device includes forming a mask (11) on the N-channel device, and etching the first glass layer from the P-channel device.

7. Claims 15 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu with evidence provided by Wolf et al. as applied to claim 13 above, and further in view of Frenette.

Claims 15 – 19 will be considered using the combination of Wu and Frenette similar to the combination of Wu and Frenette used in claims 1 – 12, above, which, for simplicity, will not be repeated here.

With regard to claim 15, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0022], wherein the first glass layer comprises phosphosilicate glass and the second glass layer comprises boron silicate glass.

With regard to claim 16, the combination of Wu and Frenette teaches in Wu, paragraph [0023], wherein the first area is an N-channel area and the second area is a P-channel area.

With regard to claim 17, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0022], wherein the forming a first glass layer includes depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å (the overlapping, disclosed range of 100 Å – 2000 Å anticipates the claimed range).

With regard to claim 18, the combination of Wu and Frenette teaches in Wu, paragraphs [0021] – [0022], wherein the forming a second glass layer includes depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å (the overlapping, disclosed range of 100 Å – 2000 Å anticipates the claimed range).

With regard to claim 19, the combination of Wu and Frenette teaches in Wu, paragraph [0023], wherein the annealing causes the fin structure in the first area to be doped with phosphorus and the fin structure in the second area to be doped with boron.

Response to Arguments

8. Applicant's previous arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N. Drew Richards
AU 2815

KENNETH PARKER
SUPERVISORY PATENT EXAMINER